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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/849,319	05/18/2004	Richard Yen-Hsiang Chang	174/311	7012

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FISH & NEAVE IP GROUP
ROPES & GRAY LLP
1211 AVENUE OF THE AMERICAS
NEW YORK, NY 10036-8704

EXAMINER	
EJAZ, NAHEED	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
08/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/849,319	CHANG ET AL.	
	Examiner	Art Unit	
	Naheed Ejaz	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8,9 and 20-22* is/are rejected.

7)☒ Claim(s) *3-7, 10-19 and 23-34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 8, 9 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (6,041,090) in view of To et al. (2003/0167417) (hereinafter, To).

3. As per claim 1, Chen teaches, 'a source of a plurality of phase-distributed clock signals (figure 2, element 22, 'Clock1-Clock5', col.3, lines 44-47); and circuitry for selecting two, phase-adjacent ones of the clock signals that currently have transitions on respective opposite sides of transitions in a serial data signal (figure 2, element 25, 'clock3, clock4', & 21B, col.2, lines 32-52, col.5, lines 66-67, col.6, lines 1-6), the circuitry separately monitoring the consistency with which each of the selected two, phase-adjacent clock signals has transitions on each side of the transitions in the serial data signal (figure 2, elements 34, 36 & 38 combined, col.4, lines 51-67, col.5, lines 1-16, col.5, lines 66-67, col.6, lines 1-6).

Chen does not teach selecting one of the selected two clock signals based on the consistency.

To teaches, 'selecting one of the selected two clock signals based on the consistency' (figures 5 & 12, page # 2, paragraphs # 0030, 0032, page # 3, paragraphs # 0033 & 0036).

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to implement the teachings of To into Chen in order to generate clock for data capture by generating a single synthesized clock between two of the selected clocks in order to accurately detect and synchronize a received data signal as taught by To (page # 2, paragraph # 0030).

4. As per claims 2, 9 & 21, Chen recovers data output 32 from data sampler 26 (figure 2) which is based on recovered clock 27 (figure 2, col.3, lines 44-50, col.4, lines 34-41).

5. As per claim 8, in addition to aforementioned rejection of claim 1, Chen teaches, 'selecting two phase-adjacent ones of a plurality of phase-distributed clock signals (figure 2, element 25, col.2, lines 32-62); comparing phases of the selected two phase-adjacent clock signals to phase of a serial data signal (figure 2, elements 25, 26 & 30, col.2, lines 32-62; and changing the selected phase-adjacent clock signals until the phases of the selected two phase-adjacent clock signals are predominantly on respective opposite sides of the phase of the serial data signal (figure 2, col.4, lines 51-67, col.5, lines 1-17) (it is noted that Chen teaches that there are two selected adjacent phase shifted clocks 'Clock 3 & Clock 4' (figure 2, col.3, lines 45-47) inputs to phase detector 34 (figure 2) and a serial data input 21B (figure 2), phase detector 34 compares the two adjacent phase shifted clock signals with input data 21B with respect

to rising and falling edges of the Clock input signals in order to align the data (col.4, lines 51-67, col.5, lines 1-17) which reads on claim limitations) , and thereafter changing the selected phase-adjacent clock signals only if a first of those signals becomes more predominantly on one side of the phase of the serial data signal than a second of those signals by a predetermined amount' (figure 8, elements 34, 94 & 104, col.5, lines 47-65) (it is noted in the mentioned columns and lines and figure 8, Chen teaches three phase detectors 34, 94 & 108 (figure 8) each with two different phase adjacent clock inputs (figure 8, elements 25, 95 & 105), the phase detectors (figure 8) compares the clock inputs with input data and change the clock signals accordingly which reads on claim limitations).

6. Claim 20 is rejected under the same rationale as mentioned in the rejections of claims 1 and 8 above. Chen does not teach circuitry for controlling phase distributed clock signals.

To teaches control circuitry which controls the phase delayed clock signals and thus phase detector 604 (figure 6, element 605, page # 2 to 4, paragraphs # 0032 & 0033) which reads on claim limitations of 'circuitry for controllably selecting two phase-adjacent ones of a plurality of phase-distributed clock signals'. To also teaches that control 605 controls the phase detector through delay elements 606A-606D and adjust the phase shifts (figure 6, page # 3, paragraph # 0033-0034) which reads on claim limitations 'circuitry responsive to the circuitry for comparing for controlling the circuitry for controllably selecting'.

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to implement the teachings of To into Chen in order to generate clock for data capture by generating a single synthesized clock between two of the selected clocks in order to accurately detect and synchronize a received data signal as taught by To (page # 2, paragraph # 0030).

7. As per claim 22, Chen teaches, 'the circuitry for comparing comprises: first and second phase detector circuitries for respectively comparing phases of the first and second selected phase-adjacent clock signals to the phase of the serial data signal' (figure 8, elements 21, 34, 94 & 104, col.5, lines 47-65).

Allowable Subject Matter

8. Claims 3-7, 10-19, 23-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Lakshmikumar (6,104,228) teaches phase aligner system and method (figure 7, col.8, lines 23-65).
- Long (5,081,655) teaches digital phase aligner and method for its operation.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naheed Ejaz whose telephone number is 571-272-5947. The examiner can normally be reached on Monday - Friday 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Naheed Ejaz
Examiner
Art Unit 2611

NE.
8/16/2007

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER